The features, nature, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

FIG. 1 is a simplified block diagram of a communications system;

FIG. 2 is a block diagram of a specific embodiment of a receiver unit suitable for receiving and processing a modulated signal;

FIG. 3 is a diagram of a data frame format for a forward link transmission in accordance with a high data rate (HDR) CDMA system;

FIG. 4 is a block diagram of an embodiment of a receive data processor that can be used to process a forward link data transmission in the HDR CDMA system;

FIG. 5 is a block diagram of a specific embodiment of a data processor of the invention;

FIGS. 6A and 6B are diagrams illustrating the writing and reading of data samples to and from a buffer, and the writing and reading of PN samples to and from the buffer, respectively;

FIG. 7A is a block diagram of a specific embodiment of a correlator within the data processor of FIG. 5;

FIG. 7B is a block diagram of a specific embodiment of a multiplier that can perform complex despreading;

FIG. 7C is a diagram that illustrates linear interpolation;

FIG. 7D is a block diagram of a specific embodiment of an interpolator;

FIG. 8A is a block diagram of a specific embodiment of a symbol demodulator and combiner within the data processor of FIG. 5;

FIG. 8B is a block diagram of a specific embodiment of a fast Hadamard transform (FHT) element;

FIG. 8C is a block diagram of a specific embodiment of a pilot demodulator;

FIG. 9 is a block diagram of a specific embodiment of an accumulator used for processing traffic data, pilot reference, and other signaling data;

FIG. 10 is a block diagram of a specific embodiment of a micro-controller that can be used to control the operation of the elements of the receiver unit; and

FIGS. 11A and 11B are timing diagrams for the processing of data samples by the data processor for time offsets of zero and 1.5, respectively.

DETAILED DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Fig. 6C is a block diagram of a specific embodiment of the data buffering for the receiver design shown in Figs 2 and 5.